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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,202	12/28/2001	Hong Sung Song	049128-5054	5389

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EXAMINER

LIANG, REGINA

ART UNIT PAPER NUMBER

2674

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DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/029,202

Applicant(s)

SONG, HONG SUNG

Examiner

Regina Liang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Figs. 1-9, page 2, line 16 to page 8, line 4 of the specification) in view of Taguchi et al (US. PAT. NO. 5,745,089 hereinafter Taguchi) and Takeda et al (US. PAT. NO. 4,651,148 hereinafter Takeda).

As to claims 1 and 17-20, Fig. 1 of the admitted prior art discloses a LCD device comprising a LCD panel (6), a digital video card (1), a controller (2) for generating a dot clock signals and a gate start pulse using the vertical and horizontal synchronizing signals, a data driver (3) and a gate driver (5). The admitted prior art does not disclose the gate driver for applying scanning signals having at least two signal voltage levels to gate lines. However, Taguchi teaches a gate driver (Y driving circuit 102 in Fig. 2) for applying scanning signals having at least two signal voltage levels to gate lines (Va1, Va2 in Fig. 1) in response to the gate start pulse (see Fig. 21). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate driver of the admitted prior art to apply scanning signals having at least two signal voltage levels to gate lines in response to the gate start pulse as taught

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by Taguchi such that the frequency band in use is narrowed, the crosstalk is reduced, and false images and flicker on the display screen can be suppressed (see the abstract of Taguchi).

The admitted prior art as modified by Taguchi does not explicitly disclose the controller generating a dual gate start pulse, and the gate driver for applying scanning signals having at least two signal voltage levels to gate lines in response to the dual gate start pulse. However, Figs. 21, 22 of Taguchi teaches the gate driver shifting the voltage output V_{a2} and V_{a1} successively to gate lines in response to the Y horizontal clock, which is the same manner as applicant to apply scanning signals having at least two signal voltage levels to gate lines in response to the dual gate start pulse. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to realize the admitted prior art as modified by Taguchi having a dual gate start pulse and the gate driver for applying scanning signals having at least two signal voltage levels to gate lines in response to the dual gate start pulse as claimed.

The admitted prior art as modified by Taguchi does not disclose the device comprising during application of a scanning signal to a pre-stage gate line, a subsequent scanning signal is applied to a gate line. However, Fig. 4 of Takeda teaches a LCD device comprising during application of a scanning signal to a pre-stage gate line, a subsequent scanning signal is applied to a gate line (the scan pulses applied between adjacent row electrodes are overlap themselves during a pulse width period). Thus it would have been further obvious to one of ordinary skill in the art at the time the invention was made to modify the device the admitted prior art as modified by Taguchi to apply a subsequent scanning signal to a gate line during application of a scanning signal to a pre-stage gate line as taught by Takeda so as provide a driving method that effectively minimizes the voltage decline caused by incomplete charge against the display picture element

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electrodes through the switching transistors, and effectively prevents possible degradation of the display characteristics (see col. 4, lines 46-55 of Takeda).

As to claim 2, Fig. 22 of Taguchi teaches the gate driver including a shift register, and a level shifter for shifting voltages having a first level and a second level different from the first level.

As to claims 3, 9, Fig. 3 of the admitted prior art teaches a storage capacitor.

As to claims 4, 10, the admitted prior art teaches the pixel voltage is a different polarity for each gate line.

As to claims 5, 11, Fig. 4 of Takeda teaches the voltage level of the scanning pulse is applied to the gate lines during at least two consecutive horizontal period signals.

As to claims 6-8, 12-16, Taguchi teaches the voltage level of the scanning pulse has at least two different levels, Takeda teaches apply the voltage level of the scanning pulse to the gate lines during two consecutive horizontal period signals. Thus, the admitted prior art as modified by Taguchi and Takeda have the voltage level of the scanning pulse during a second horizontal period signal is larger than or more than twice the voltage level of the scanning pulse during the first horizontal period signal as claimed.

Response to Arguments

3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

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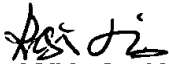
4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (703) 305-4719. The examiner can normally be reached on Monday-Friday from 9AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.


REGINA LIANG
PRIMARY EXAMINER
ART UNIT 2674

RL
4/9/04